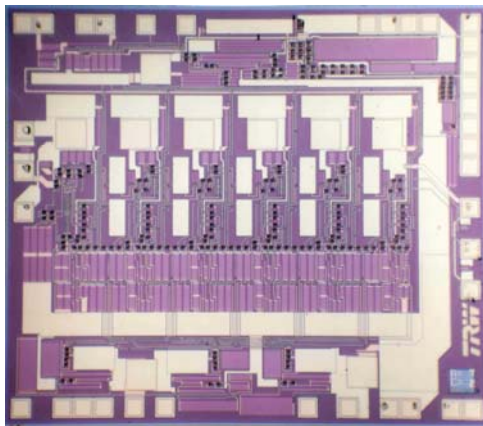




Features

- ◆ RF frequency: 0.12 to 1.35 GHz
- ◆ Extended Dynamic Range:
-65 to +5 dBm
- ◆ Fast Rise Time: 15 ns
- ◆ Rapid Fall Time: 22 ns
- ◆ Superior Delay Time: 2 ns
- ◆ Excellent Linearity
- ◆ Die Size: < 5.1 sq. mm



X=2450µm Y=2075µm

Description and Application

The AEB101C monolithic HBT MMIC is applicable for operation in high precision systems that require outstanding pulse performance, high sensitivity, and low DC power consumption. Along with superior performance, it is the industry's smallest GaAs SDLA for your ECM, or monopulse receiver designs. This, coupled with lower cost through volume production, provides the optimum solution for your EW channelized receiver, communications receiver, compressive receivers, and IF strip applications.

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
RF Frequency	0.12		1.35	GHz
Logging Range		65		dB
Tangential Sensitivity	-65	-70		dBm
Input Return Loss	10	13		dB
Log Output				
Linearity		±0.8	±1.2	dB
Slope		30		mV/dB
Rise Time	15	18	25	ns
Fall Time		-12		ns
Limited RF Output		-12		dBm
DC Power				
-5V Current		150		mA
+5V Current		40		mA
Temperature Rise Junction to Back of Flat Pack				°C

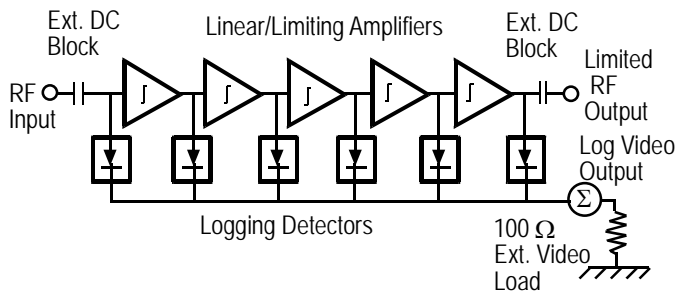
Absolute Maximum Ratings (Ta = 25°C)
With 100 Ohm Video Load

Parameter	Min	Max	Unit
RF Input Power		14	dBm
Positive Supply		5	V
Negative Supply		-5	V
Operating Temp		110	°C
Storage Temp		125	°C
Ext. Video Load, Min.		95	Ohms

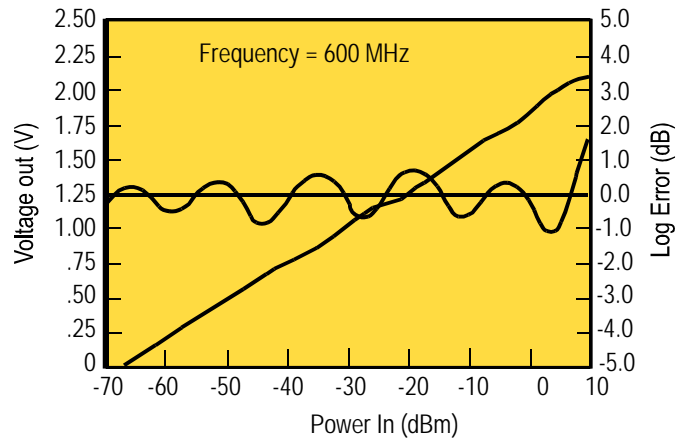
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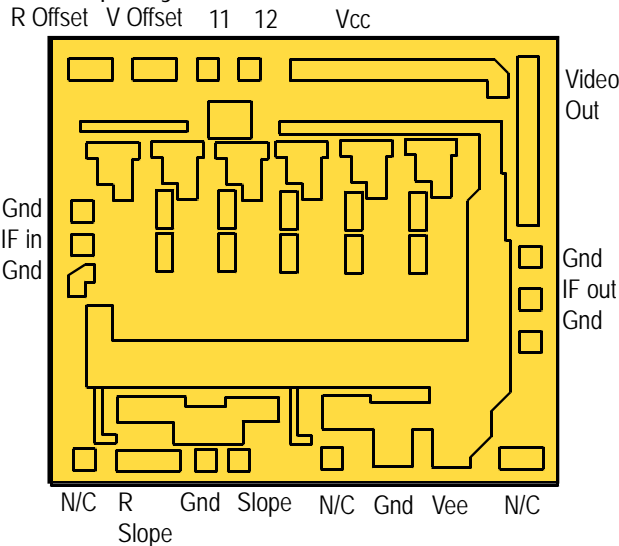
Circuit Topology



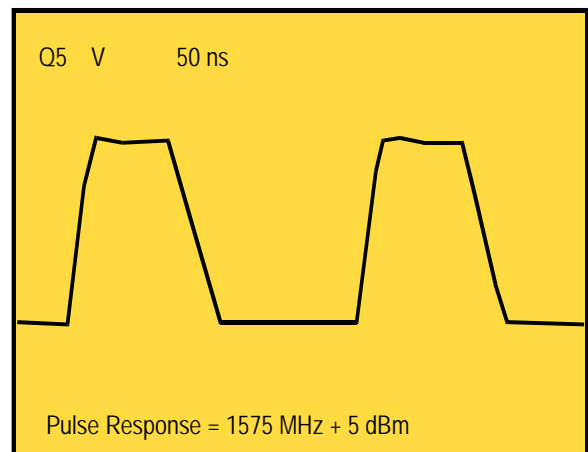
Dynamic Range and Log Error



Chip Layout



Pulse Response



Pulse Response for 1575 MHz signal,
+ 5 dBm ON, -60 dBm OFF Power

9800202 1902a-NT

Recommended Assembly Notes

- External DC blocks required.
- Log slope can be externally adjusted.
- Offset voltage can be externally adjusted.
- 4 Mil thick chip with backside via grounds
- 1000pF chip capacitors are required on DC bias lines

Device Power Up Instructions

1. Make sure Vcc = 0, Vee = 0.
2. Bias up Vee to - 5 V first; no constraint on ramping up the voltage, fast turn on is preferred.
3. Bias up Vcc to + 5 V next; again fast turn on is preferred. It is lower risk to first bias up Vee and then Vcc.

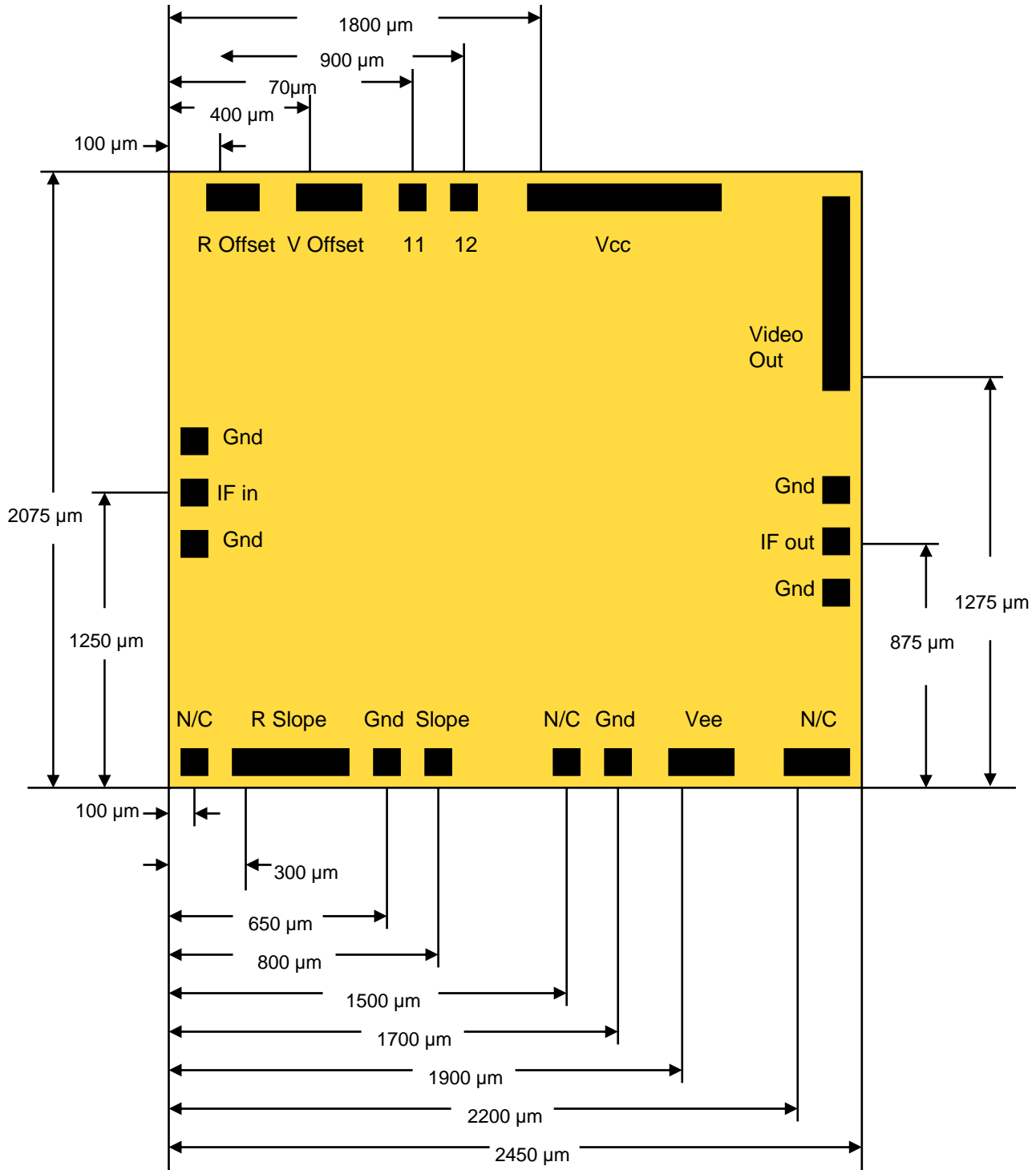
Device Power Down Instructions

1. For best results, reverse the sequence identified above in steps 1 through 3.

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Die Size and Bond Pad Locations



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